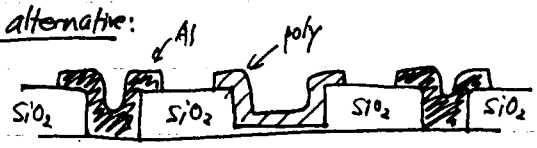
Isolation Technologies

LOCOS → why?
- Must prevent inversion in the field regions.
- LOCOS is used as opposed to other isolations because of its smooth topography.

Consider the simplest alternative:



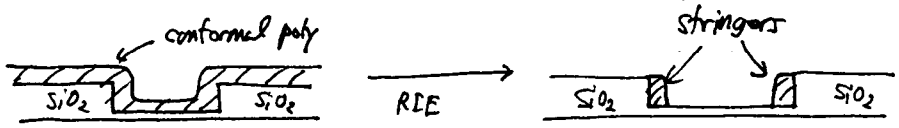
(ideal goal)

→ but in reality, topography will greatly limit what can be done

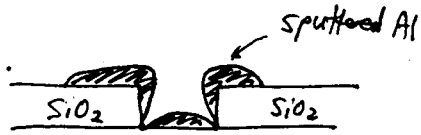
⇒ Some of the problems due to topography:

① Lithography: PR step coverage problems + stepper focusing

② Stringers after anisotropic etching:



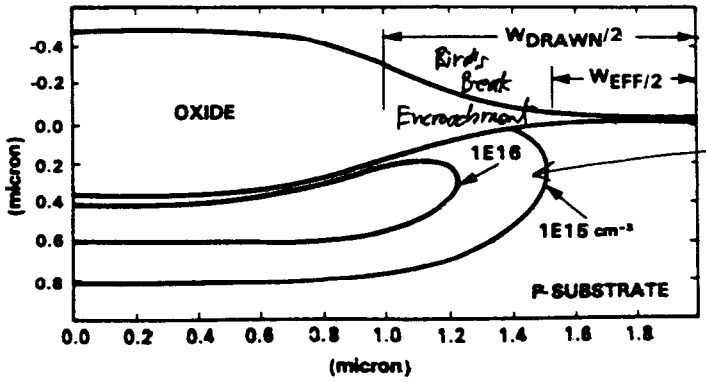
③ Metal step coverage problems:



⇒ LOCOS solves all of these problems.

⇒ But LOCOS introduces several problems of its own: (at least conventional semi-recessed LOCOS does)

① Bird's beak encroachment into active areas: for 0.5–0.6 μm F.O. → 0.5 μm/side encroachment (thus, 1μm features would disappear!)



Channel-stop Implant Encroachment

Fig. 15.1

Channel widths are particularly limited by LOCOS encroachment:

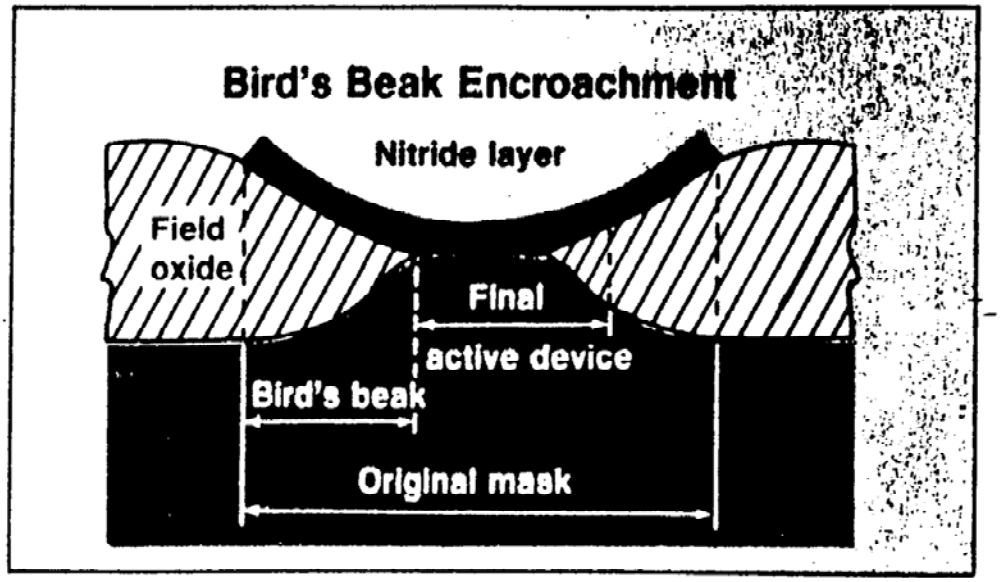


Fig. 15.2

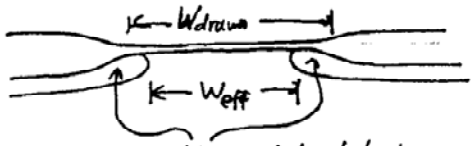
② Excessive redistribution of channel-stop implant.

⇒ especially problematic w/ B → get oxidation-enhanced diffusion

→ implant dose must be heavy and deep

can cause high S/D-to-substrate junction capacitance & lower junction breakdown voltage

⇒ get narrow width effects due to channel-stop implant encroachment, as well (See Fig. 15.1 again)



V_t raised due to high channel-stop implant concentration } ∴ the width is effectively reduced

⇒ partial solutions:

(i) high pressure oxidation (HIPOX): grow LOCOS @ lower T → less diffusion of dopants

(ii) use Ge-B co-implant: B diffusivity lower in presence of Ge

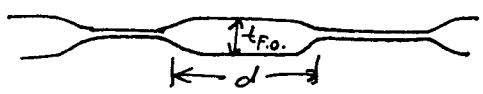
(iii) use a Cl implant: oxide grows at a faster rate → less time-temperature ∴ smaller Dt.

③ Planarity of LOCOS becoming inadequate for submicron needs.

⇒ stepper lithography has problems focusing over excessive topography

⇒ the smaller the dimensions → the smaller the allowable topography

④ Thickness in closely spaced regions less than in open areas.



For $d = 1.5\mu m \longrightarrow t_{F.O.} = 4000Å$

$d = 0.8\mu m \longrightarrow t_{F.O.} = 2900Å$

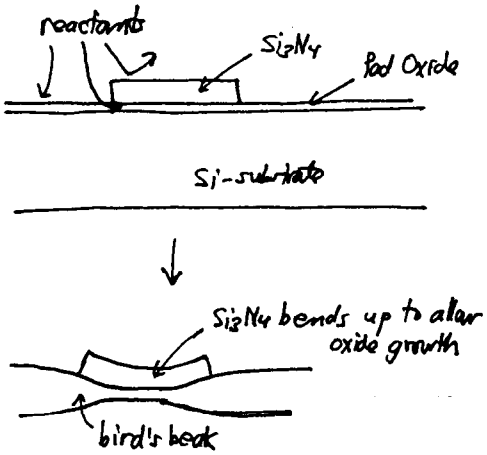
⇒ caused by reduction in oxidants available in submicron openings.

⇒ minimum space (d) allowed: $0.75\mu m$ for 5500Å thick oxide

Advanced Semi-recessed Oxide LOCOS Isolation Processes

Question: why the long bird's beak?

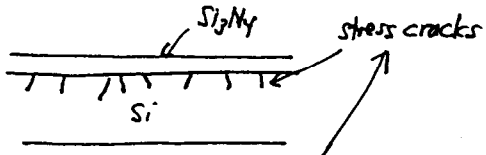
⇒ lateral diffusion of reactants under the nitride mask:



⇒ the finite pad oxide thickness allows lateral diffusion of reactants

⇒ w/o this oxide, there would be no bird's beak

So why the pad oxide? Why not get rid of it?



⇒ if deposit Si_3N_4 directly on SiO_2, get stress cracks in the Si → degrades MOS Xistors!

⇒ thus, need pad oxide:

$t_{pad\ oxide} \sim 200Å - 600Å$

as $t_{Si_3N_4} \uparrow \longrightarrow$ stress cracks ↑

↓

yield ↓

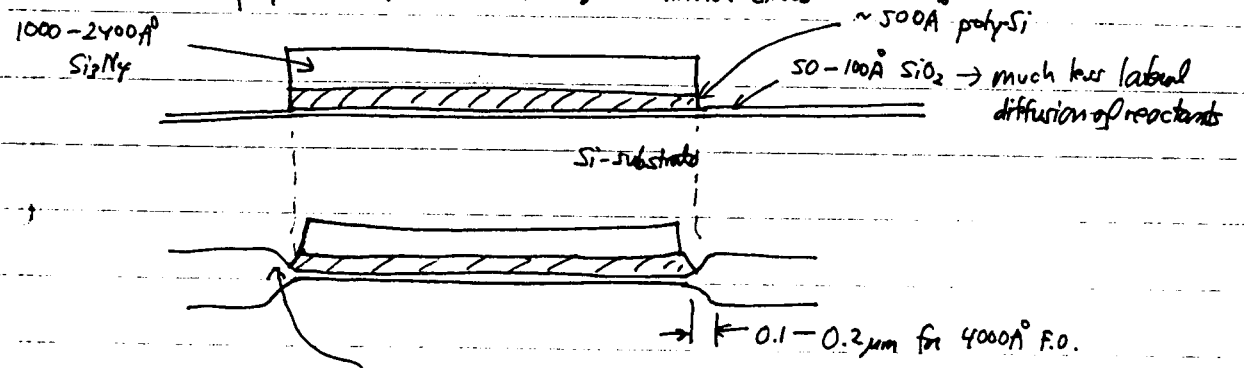
MOS performance ↓

There are methods, however, by which the pad oxide thickness can be reduced:

① Polybuffered LOCOS

⇒ poly does not induce as much stress as nitride

⇒ use a poly-oxide layer to buffer against nitride stress



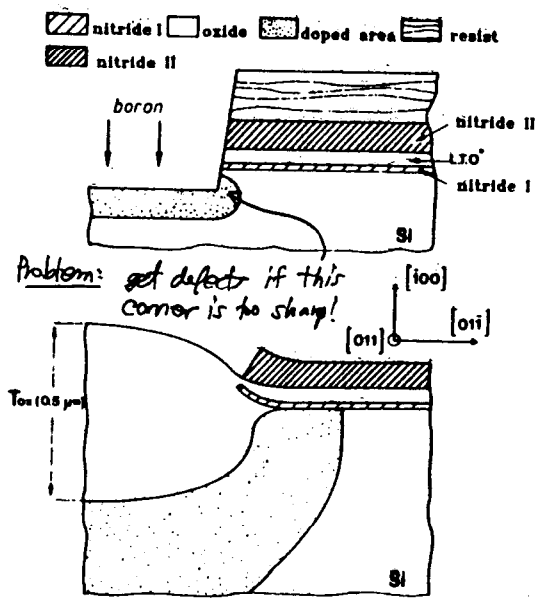
Problem: higher step → this is a problem

Problem: doesn't reduce channel-stop implant encroachment

⇒ possible solution for submicron devices: grow thinner F.O. (~2200Å thick) and implant heavier channel-stop doping conc.

⇒ ok for submicron, since heavier doping needed for punchthrough reduction anyway.

② Sealed-Interface Local Oxidation (SILO)



*LTO = low temperature oxide

Process:

① From 100–200Å nitride layer directly on Si by thermal nitridation of Si, or by CVD.
→ thin nitride layer reduces edge stress
∴ reduces # of defects

② LPCVD SiO_2: 250 – 300Å

③ LPCVD nitride: 1500 – 2000Å film

} 3-layer masking film

④ Pattern 3-layer masking film via RIE
⇒ get some etching of Si

⑤ Grow F.O. ⇒ get some lateral encroachment of F.O. due to

⑥ channel-stop implant

Fig. 15.3

⇒ net result: very little lateral oxide growth → very little LOCOS encroachment

⇒ Bird's beak length ~ 0.2 μm → caused by overetch into Si @ step (4)

Summary:

Above two processes work due to less lateral oxide growth as pad oxide thickness ↓

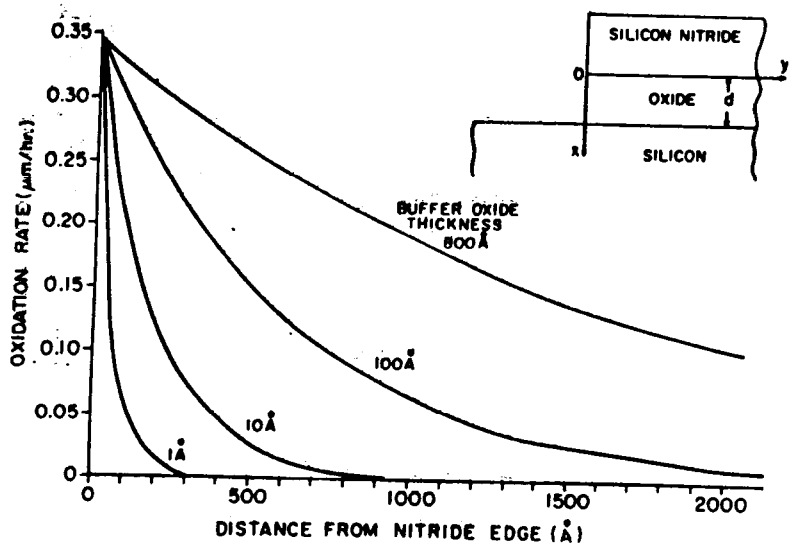


Fig. 15.4

But both of the above processes also suffer from steps that are too abrupt

→ for submicron processes (where steppers are involved in lithography), such steps must be eliminated.

Thus:

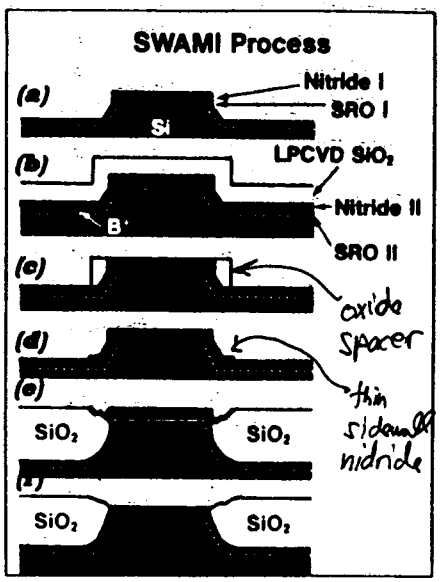
Fully Recessed Oxide LOCOS Isolation Processes

⇒ LOCOS process, but w/o the Bird's head

↳ decreased topography

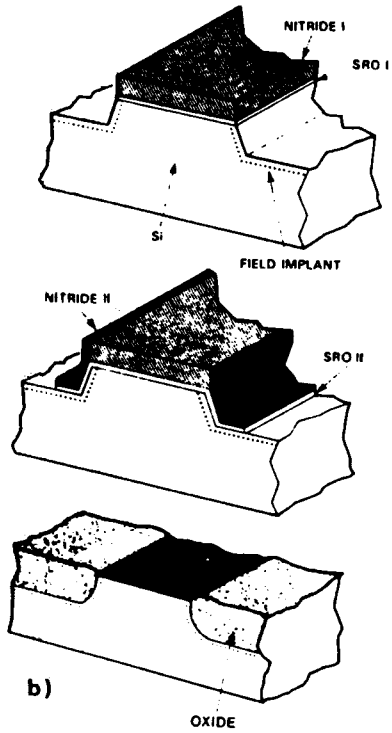
→ less lateral oxide encroachment in some cases

Sidewall-Masked Isolation (SWAMI)



SRO = Stress-relief oxide

a)



b)

Fig. 15.5

Process Flow:

① Pad oxidation and LPCVD nitride as in conventional LOCOS process. [(a) in Fig. 15.5]

② Etch grooves into Si (usually via an orientation-selective silicon etch, such as KOH)

↳ results in sidewalls w/ 66° incline when starting wafer is <100>

⇒ this reduces stresses when growing F.O. → reduces edge defects

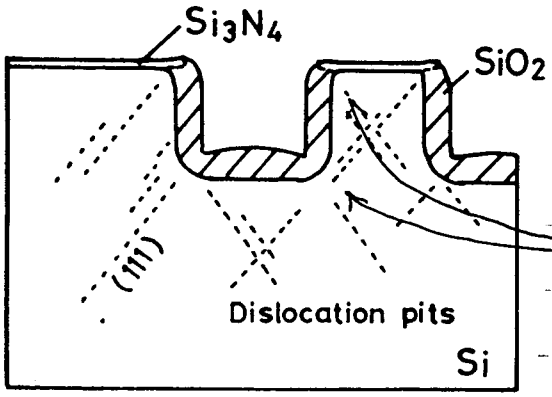


Fig. 15.6

Edge defects generated at corner points (high stress field points)

→ also, high E field at corners for MOS devices → get lower V_t's if corner is too sharp → thus, get excessive leakage current ∴ It is necessary to round the corners!

③ Grow second stress relief oxide.

④ Deposit second CVD nitride → conformally covers all steps.

⑤ Deposit CVD oxide → again, conformal coverage : [(b) in Fig. 15.5]

⑥ Anisotropic etch of HTO/Si_3N_4/thermal SiO_2 layer down to Si in the field regions
→ Si_3N_4 remains over active areas and under oxide spacers. [(c) in Fig. 15.5]

⑦ Etch away oxide spacer (wet etch) [(d) in Fig. 15.5]

⑧ Channel-stop implant.

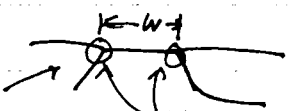
⑨ Grow field oxide → thin nitride sidewall (step) bends up [(e) in Fig. 15.5]

⑩ Remove nitride/oxide layers. [(f) in Fig. 15.5]

Result: very planar isolation w/ excellent topography.

Problems: ① More complex than conventional LOCOS.

② Corner effects → V_t lowering at device edges
→ must round corners as much as possible



③ More common effects: dislocations, defects

Self-Aligned Planar-Oxidation Technology (SPOT)

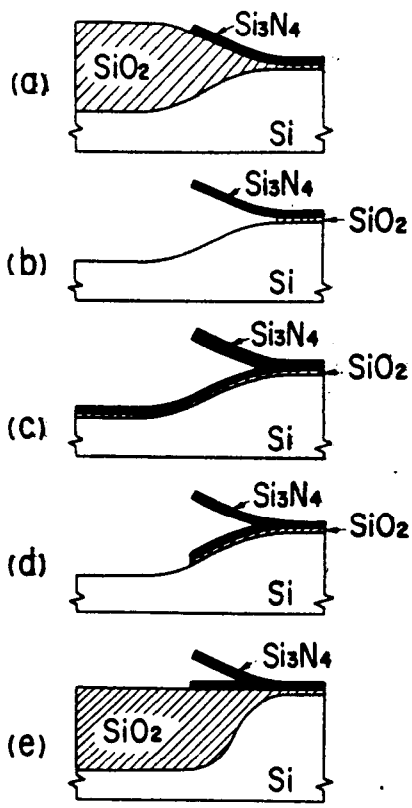


Fig. 15.7

Process Flow:

① Standard LOCOS. [(a)]

② Isotropic oxide etch w/ buffered HF solution. [(b)]

③ Pad oxidation.

④ LPCVD nitride → conformal deposition [(c)]
→ thinner than first nitride layer

⑤ Anisotropic etch → new nitride shadowed by original LOCOS nitride. [(d)]

⑤a Channel-stop implant.

⑥ High pressure Field Oxidation @ 900°C. [(e)]
↗ low T → less channel-stop implant encroachment.

Problem: still get oxide encroachment!

Fully Recessed Oxide (FUROX)

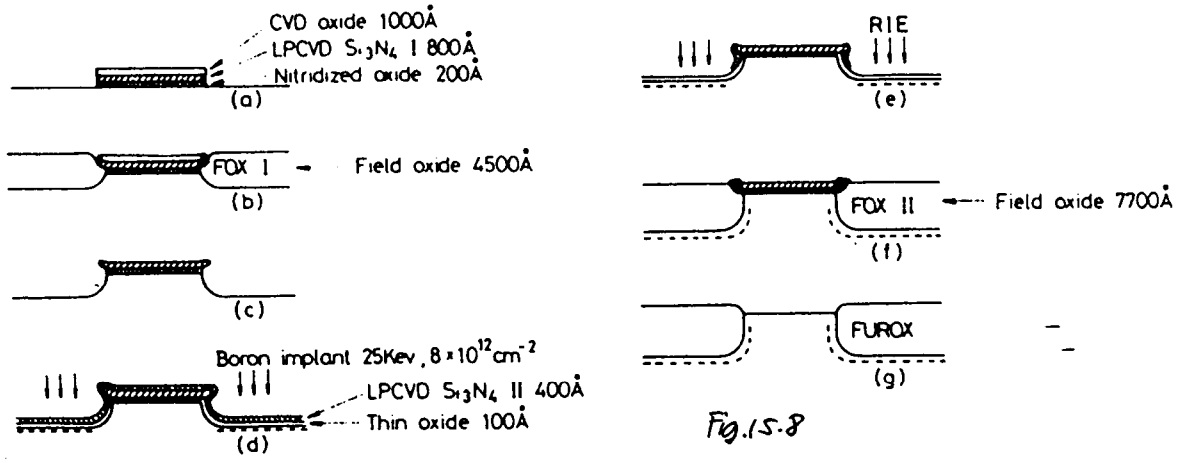


Fig. 15-8

Process Flow:

① Minimum-encroachment LOCOS (using a method detailed previously, a using a nitridized oxide, as shown above) [(a) & (b)]

Nitridization: ← impedes Bird's beak encroachment
① grow oxide
② 1200°C for 7 hrs. in NH_3

② Etch away the first field oxide. [(c)]

③ Grow 2nd pad oxide → 100Å.

④ LPCVD Si_3N_4 → 400Å.

⑤ Channel-stop implant. [(d)]

⑥ Anisotropic etch of 2nd pad oxide and nitride (RIE). [(e)] (Vertical oxide/nitride stays intact due to shadowing by 1st nitride.)

⑦ Grow field oxide [(f)]

Result: good planarity, defect-free, fully recessed oxide

Bird's beak ~ 0.15 μm
Isolation width ~ 1.1 μm
} for 7700Å-thick F.O.

OSELO II

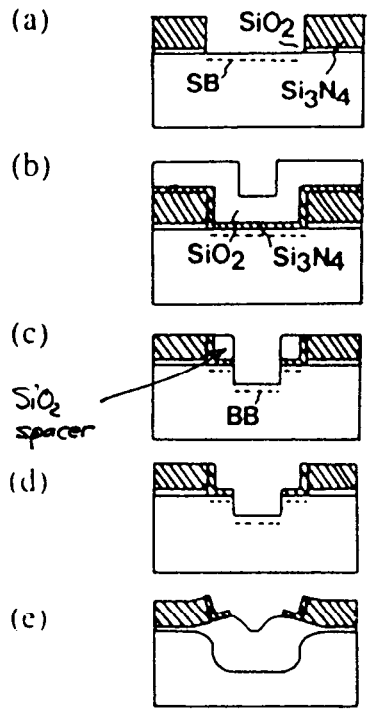


Fig. 15.9

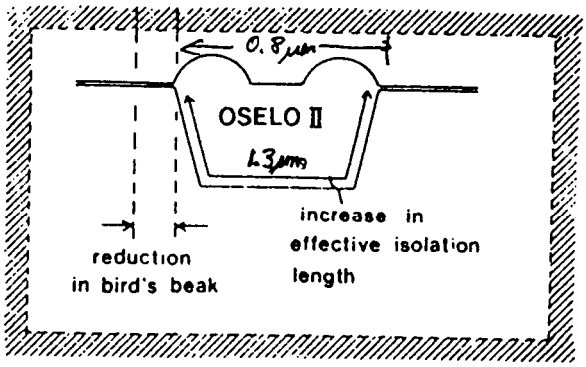


Fig. 15.10

Process Flow:

1. Standard LOCOS oxide/nitride mask layer formation and patterning → 500Å oxide, 2400Å CVD nitride
2. First channel-stop implant. → (a)
3. 2nd LPCVD nitride → 300Å-thick.
4. LPCVD oxide → 2000Å-thick → (b)
5. RIE 2nd oxide and 2nd nitride (anisotropic etch).
6. RIE Si ~ 0.2 μm deep. (oxide spacer serves as mask)
7. 2nd channel-stop implant. (for bottom of "trench") → (c)
8. Wet etch remaining SiO_2 spacer. → (d)
9. Grow 5500Å of field oxide → wet O_2, 120 min. @ 1000°C

Result: isolation length ~ 0.8 μm
effective isolation length ~ 1.3 μm (Fig. 15.10)

Problem: Si is RIE etched → sharp corners → get dislocation defects during oxide growth

Trench Etch and Refill Isolation Technologies

Main applications:

① Replacement of LOCOS for isolation of like devices within the same tub in CMOS. (shallow trench)

② Isolation of n-channel from p-channel devices → preventing latchup in CMOS. (moderate-depth to deep trenches)

③ High packing density trench capacitors in DRAMs. (deep trench)

3 Trench categories:

① shallow → < 1μm deep

② moderate-depth → 1-3 μm deep

③ deep narrow → > 3μm deep, < 2μm wide

Main advantage: no LOCOS-induced bird's beak ∴ higher packing density

Shallow Trench and Refill Isolation

Buried-Oxide Isolation (BOX) -

⇒ much easier to implement than the deeper trenches → good for devices within the same tub

⇒ but much less effective against latchup ∴ must use another isolation method for latchup protection.

Process Flow: (unadjusted BOX flow)

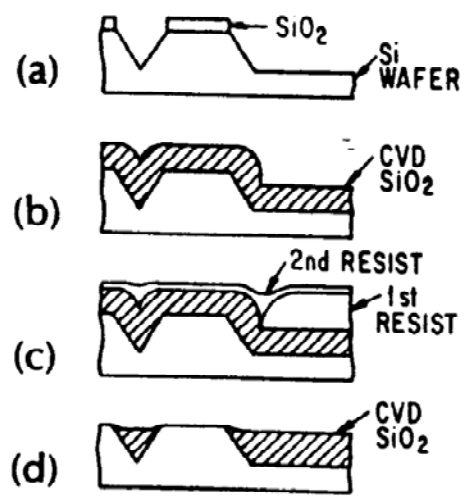
① Anisotropic etch (RIE) → 0.5-0.8 μm deep into Si substrate → (a)

② Deposit CVD oxide. → reduces dislocation defects. → (b)

③ Etch back → two options:

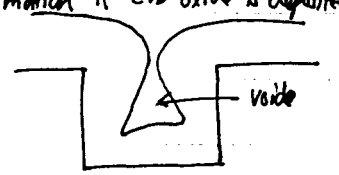
(i) Apply double layer resist to planarize the surface (first layer reflowed), then etch back in etchant that etches PR and SiO_2 at same rate (usually an RIE) → (c), (d)

(ii) Use chemical-mechanical polishing (CMP)



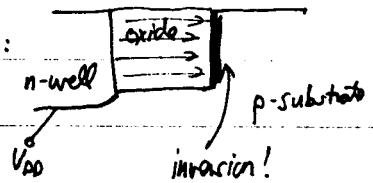
Problems w/ BOX Isolation -

① Void formation if CVD oxide is deposited in a trench narrower than 2μm.

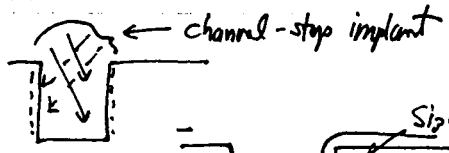


Solution: use higher temp CVD oxide or slope the sidewalls a bit

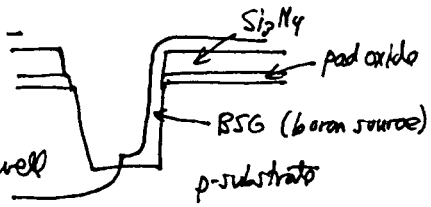
② Inversion of Si at sidewalls:



Solution: (i) shallow angle implant:



(ii) use doped oxide as diffusion source:
(pattern to get B diffusion only on p-side)

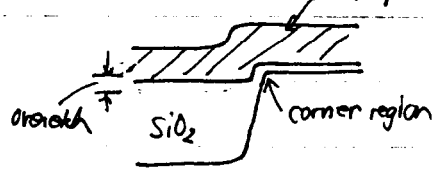


③ Varying field-oxide thickness over different areas (e.g., CVD oxide thicker over narrow areas than wider areas).

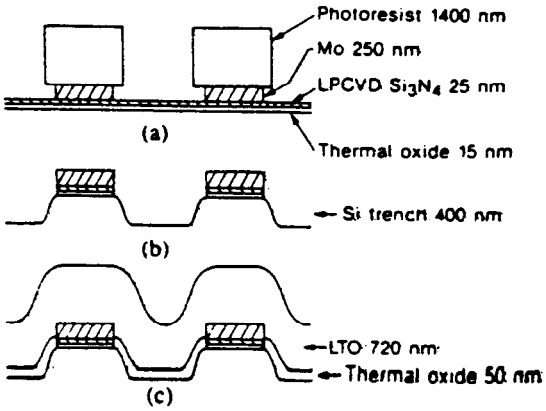
Solution: additional masking step

④ Overetch needed in the planarization step → creates corners in the Si → leads to high E-field regions → lower V_t's in MOS corners → leakage current

(due to nonuniformity of field oxide thickness across wafer)



Solution: use an etch-stop ⇒ BOXES process:



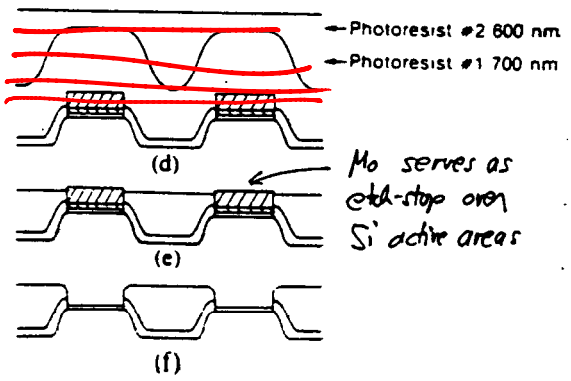
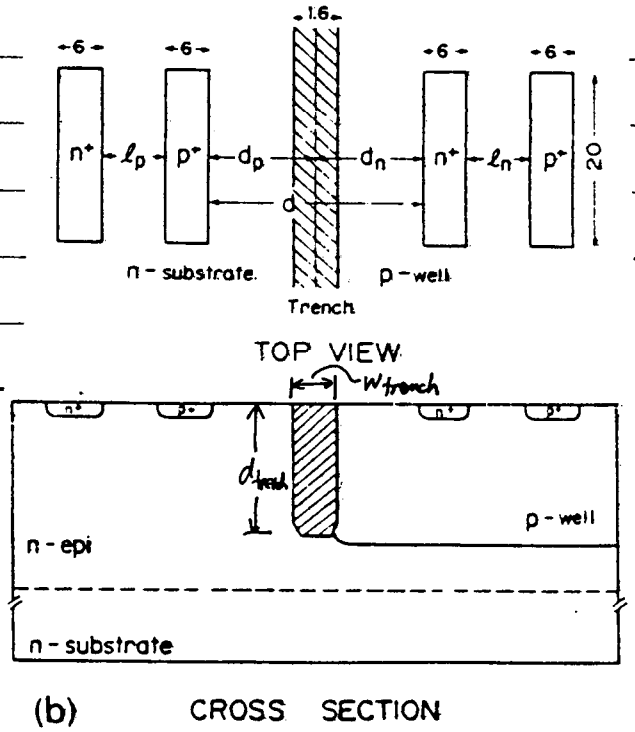


Fig. 15.12

Moderate-Depth Trench Isolation for CMOS



⇒ shallow epi layer and shallow trenches (greatly reduces complexity of trench etch and refill)

Process Flow:

① Form p-well region.

② Dry etch moderately deep trench at boundary of n- and p-regions.

③ Refill w/ polysilicon.

④ Etch back to give a planar surface.

Fig. 15.13

For $d_{trench} = 2.5\,\mu m$, $W_{trench} = 1.6\,\mu m \Longrightarrow d = 2\,\mu m$ (n^+ to p^+ spacing).

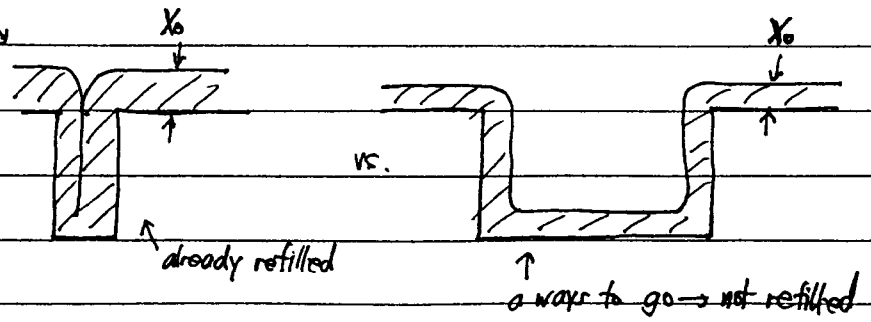
For $d_{trench} = 1.4\,\mu m \Longrightarrow d = 5.8\,\mu m$

Main Application: prevent latchup and isolate n^+ and p^+ regions

Problem: Poly trench refill process does not allow trenches of varying widths

⇒ thus, this technique is really only useful for

⇒ must utilize another method to isolate devices in a common well



Deep, Narrow Trench and Refill

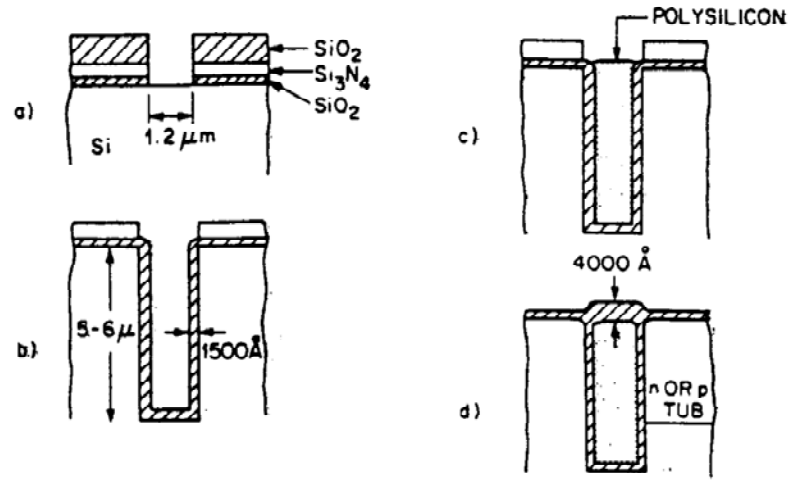


Fig. 15.14

Process Flow:

① Grow/deposit $SiO_2/Si_3N_4/SiO_2$ layer. → need extremely high Si : mask selectivity
→ masking layer that must hold up to a deep RIE Si etch.
→ hard mask: minimizes undercutting when etching

② RIE etch the silicon.

⇒ Key requirements: (i) smooth, tapered sidewalls w/ ~87° angle → allows easier refill w/ no voids

(ii) high Si : mask selectivity and no undercutting of mask

(iii) undamaged sidewalls → damage will induce leakage currents & inversion in MOS devices.

(iv) smooth trench bottom → minimizes stress-induced defects that can form after oxide growth

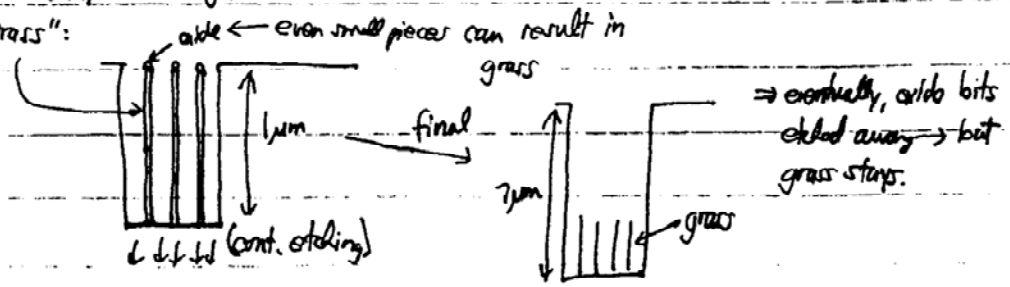
(v) trench depth should be uniform across the wafer and from wafer-to-wafer

Thus, for this etch:

(a) pattern the $SiO_2/Si_3N_4/SiO_2$ layer.

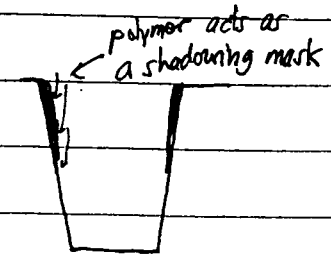
(b) remove native oxide over Si (HF dip) ← extremely important, since the RIE to be used will be have $S_{Si/oxide}$ = huge ≈ 70

↳ if not done, then can get "grass":



(c) Etch using a high density ECR or inductively-coupled plasma → high selectivity
→ high etch rate

⇒ use "surface inhibitor" RIE chemistry (Cl_2)
↳ deposit polymer on sidewalls to prevent undercutting
↳ also to promote tapered sidewalls:



⇒ For trench uniformity across the wafer, must use only one width for trenches → this is a major limitation.

(d) Change RIE to isotropic plasma etch at the bottom of trench → for rounded, smoother corners
↳ (SF_6 chemistry)

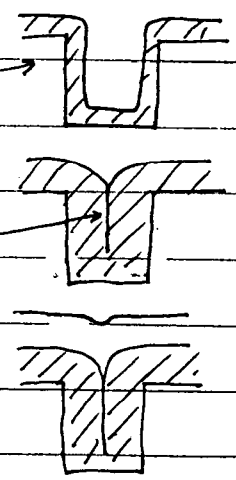
③ Grow 500Å oxide → removes Si damage caused by high energy ion bombardment during RIE trench etching.

④ LPCVD oxide → thick for isolation, thin for capacitors

⑤ Refill trench w/ polysilicon.

4 stages:

(i) Initial conformal stage.
(ii) Seam-formation stage.
(iii) Seam-closure stage.
(iv) Cusp planarization stage.



⑥ Planarize: CMP or resist+etchback.

Advantages of Deep, Narrow Trench & Refill:

⇒ very high packing density due to small n+ to p+ separation, even on standard Si wafers (i.e., don't need epi on heavily-doped substrate) → can get 1μm-wide trenches

⇒ can eliminate latch-up w/ epi on heavily-doped substrate

Problems: (i) complexity ← major problem for isolation, but worth it for DRAMs.
(ii) only one width allowable for uniform result

Selective Epitaxial Growth (SEG) Isolation

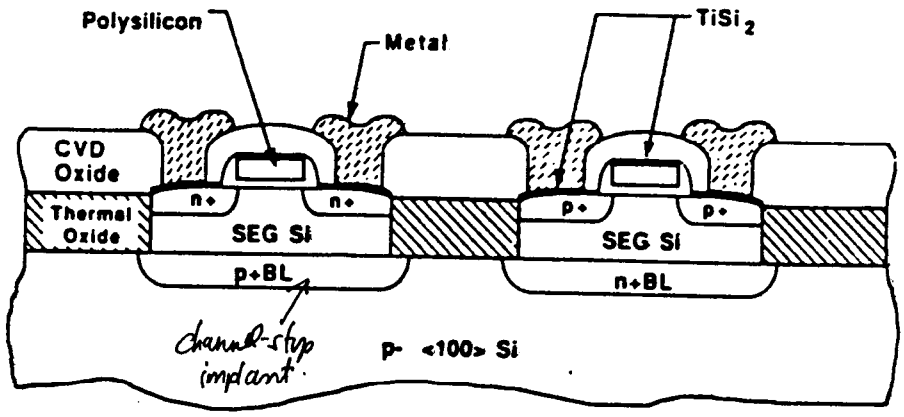


Fig. 15.15

Basic (Simplified) Process Flow:

1. Grow thermal oxide over Si substrate.
2. Pattern and RIE etch oxide down to Si to form active areas.
3. Channel-stop implant.
4. Fill trenches using SEG.
5. Process CMOS.

Advantages: (i) no bird's beak

(ii) F.O. thickness does not depend upon width of the space.

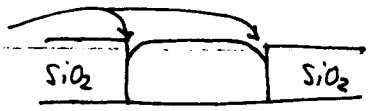
(iii) planar Si surface (except for facets — see below)

(iv) channel-stop implant removed from S/D regions → less C_j

(v) can be used for all levels of isolation: latchup prevention as well as isolation between devices in the same tub.

(vi) can use contacts that fill up the drain & source (LOCOS no longer a limitation)

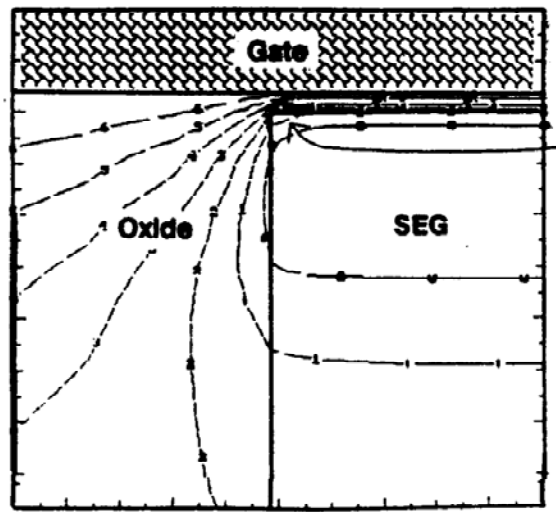
Drawbacks: (i) Facets



⇒ result in bad topography

Solution: CMP

(ii) Sharp corner effects → high E-field at corners → low V_t in these regions → increased leakage currents

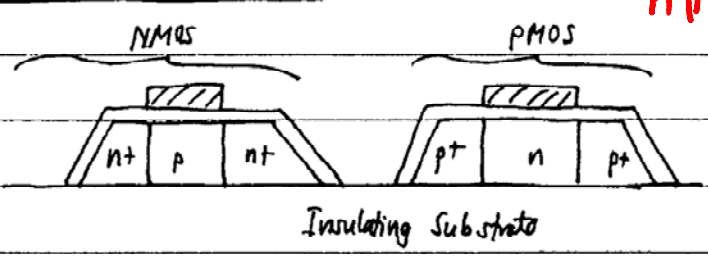


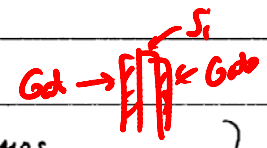
very high E-field!

Fig. 15.16

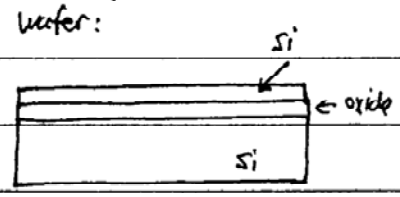
(iii) Leakage due to sidewall inversion → Solution: raise substrate-doping
(it'll have to be done anyway for submicron devices)

Silicon-On-Insulator (SOI) Isolation





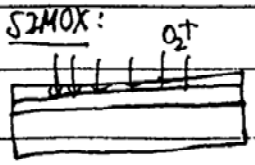
Basically, start w/ SOI wafer:



Advantages: ① C_j reduction → faster devices!
② Much higher density possible → density limited by lithography and etching
(not by latchup, oxide encroachment, etc...)
③ Eliminates latchup

Disadvantages: ① Wafer cost → but always getting cheaper w/ time.
② Poorer silicon quality due to manufacture process of SOI wafers.
⇒ but the quality is getting much better!

SIMOX:



① implant O_2^+
② anneal to form SiO_2
② epi to increase usable Si thickness